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**Class Group: COMP1D-Y**

**Lab 9 – Latches and Memory**

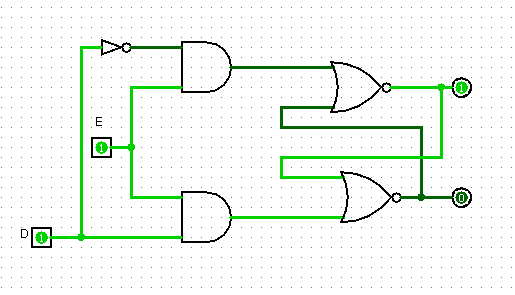
1. Describe, using your own words, a D Latch. Illustrate how it is implemented below and confirm its operation using the simulator. Draw its truth table.

**Description:**

When deactivated, D latches serve as 1-bit memory circuits, storing either a "high" or "low" state and "reading" fresh data from the D input when enabled. D latch is similar to an S-R latch, however it only has one input: "D." The circuit is set when the D input is activated, and it is reset when the D input is off. Of course, this only works if the enable input (E) is also turned on. Otherwise, the output(s) will be latched, meaning they won't respond to changes in the D input.

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| E | D | Q(T+1) |
| 0 | 0 | Qt |
| 0 | 1 | Qt |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Circuit:**

1. Show a circuit which can be used to write to a 5x4 memory. Illustrate how it is implemented below and confirm its operation using the simulator. (You may use the blackbox decoder in Logisim).

**Description:**

The user can seek up the output value for a specific input combination by using memory to conduct logic (address). Each data bit correlates to an output value, and each address corresponds to a row in the truth table.

**Circuit:**

